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NASA Case No. MDC - 2/48/-/ Print Figure

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(MASA-Case-MSC-21481-1) PROGRAMMABLE REMAPPER WITH SINGLE FLOW ARCHITECTURE Patent Application (NASA) 24 p

N91-13390

Unclas 63/60 0321050 MSC-21481-1 Serial No. 07/506,136

Filed: March 30, 1990

## **AWARDS ABSTRACT**

ISC-21481-1

## PROGRAMMABLE REMAPPER WITH SINGLE FLOW ARCHITECTURE

The invention relates in general to image processing systems and methods and in particular to a machine which accepts a real time video image in the form of a matrix of picture elements (pixels) and remaps such image according to a selectable one of a plurality of mapping functions to create an output matrix of pixels. Such mapping functions, or transformations, may be any one of a number of different transformations depending on the objective of the user of the system.

The system remaps input images from one coordinate system to another using a set of look-up tables for the data necessary for the transform. The transforms, which are operator selectable, are precomputed and loaded into massive look-up tables. Input pixels, via the look-up tables of any particular transform selected, are mapped into output pixels with the radiance information of the input pixels being appropriately weighted. An earlier embodiment of the system included two parallel processors: a collective processor which mapped multiple input pixels into a single output pixel and an interpolative processor. The interpolative processor performed an interpolation among pixels in the input image where a given input pixel may affect the value of many output pixels.

The present invention provides several advantages over previous embodiments in that the two distinct processors are replaced by a single processor capable of performing both types of operations (collective and interpolative) with no more complexity.

Previously, there has existed no image processor or "remapper" that can operate with sufficient speed and flexibility to permit investigating different transformation patterns in real time.

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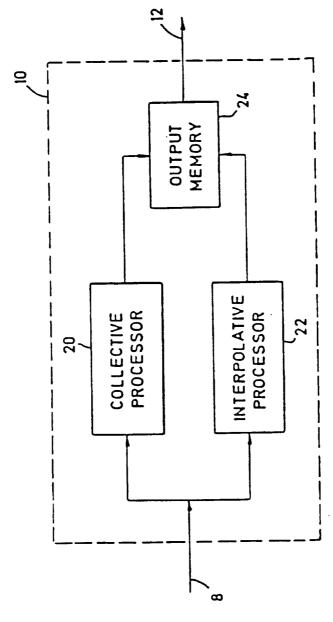
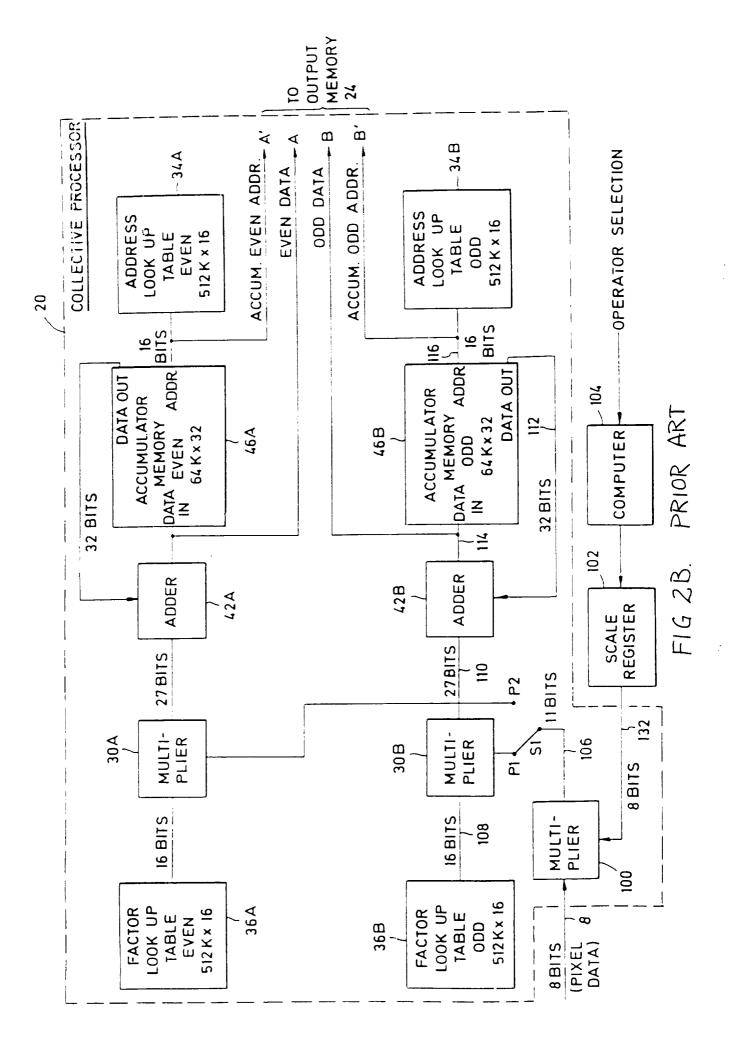
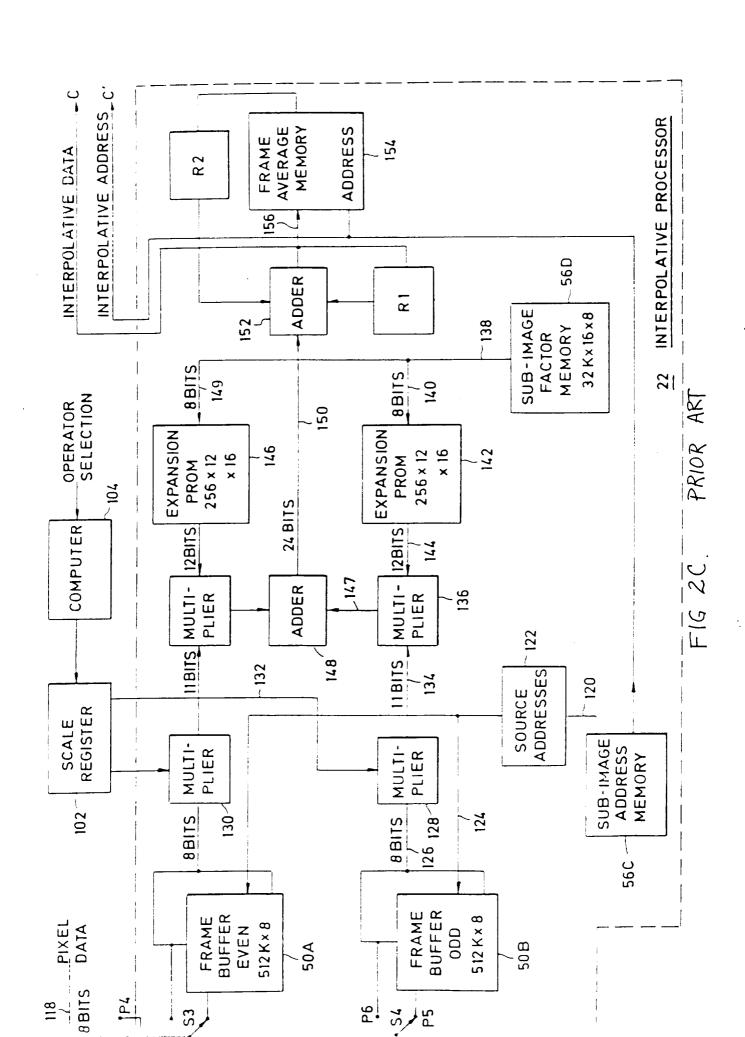
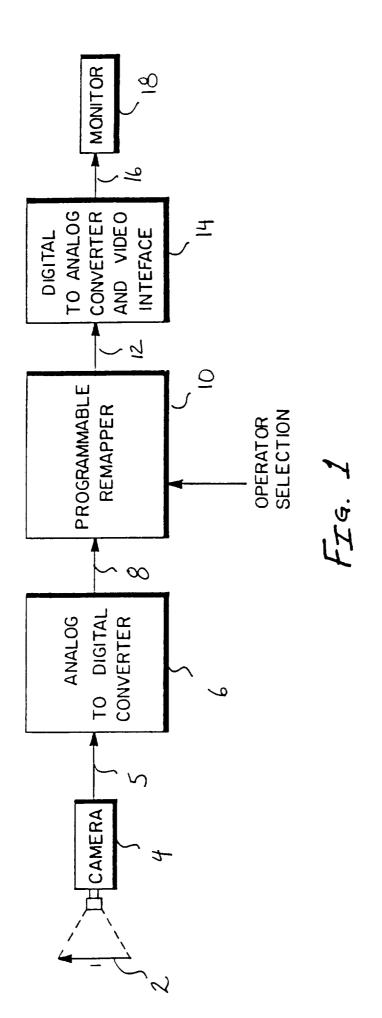
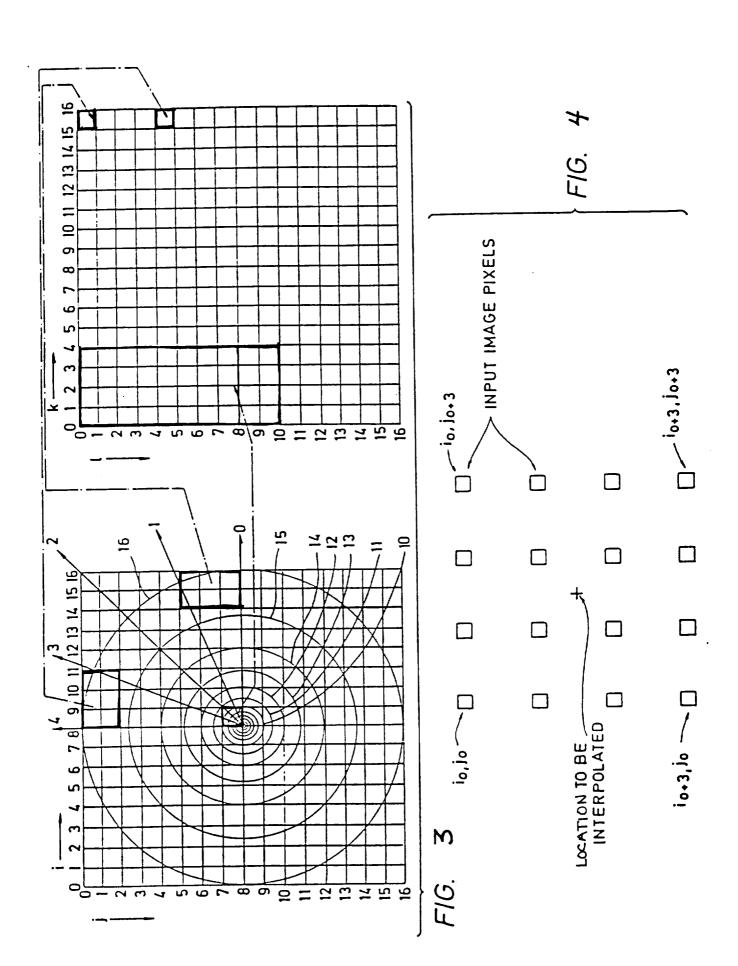


FIG. 2A PRIOR ART









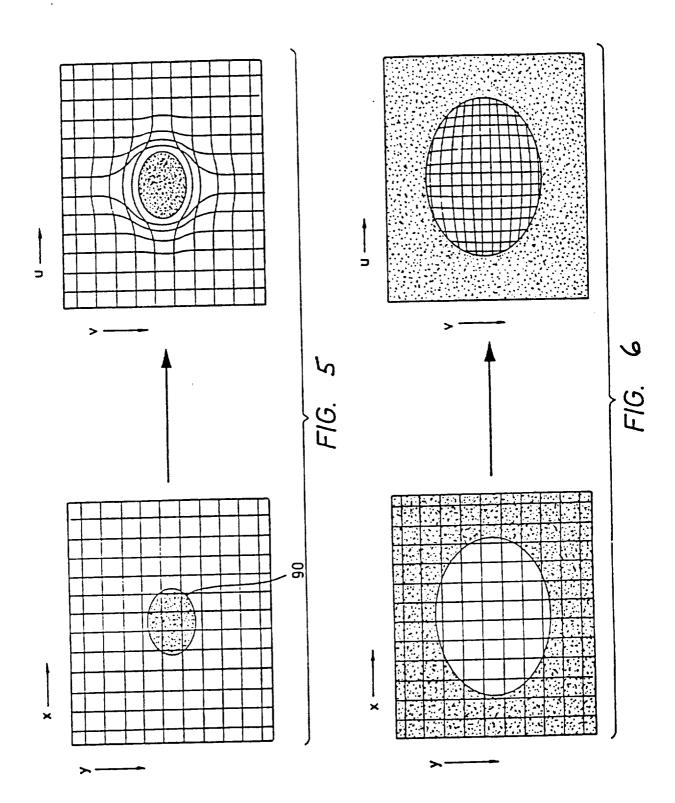


FIG.7G FIG.7B FIG. 7A CENTERED FIG.7D FIG.7C FIG. 7F FIG. 7E

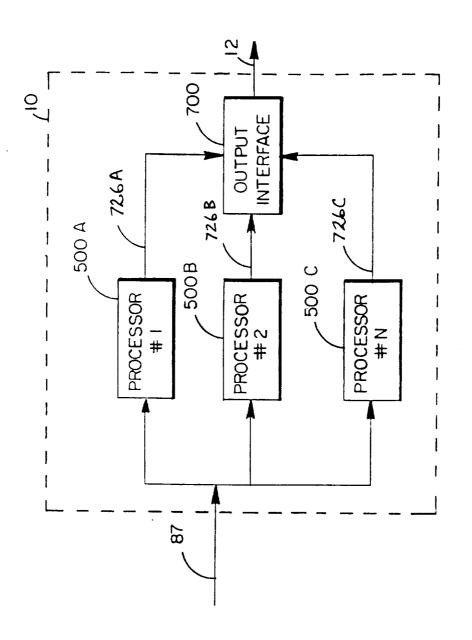


FIG. 8

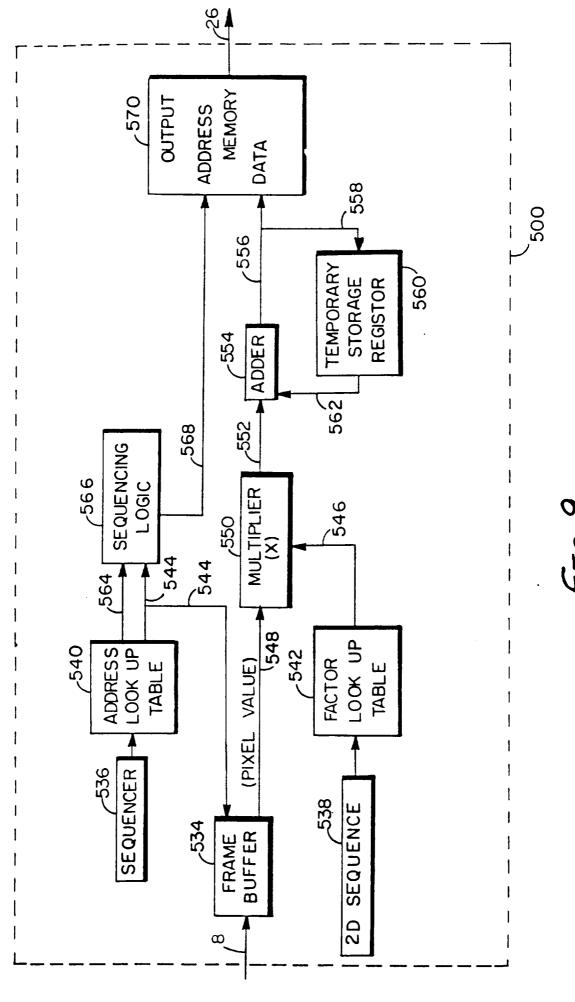


FIG. 9

FIG. 10

FIG. 11

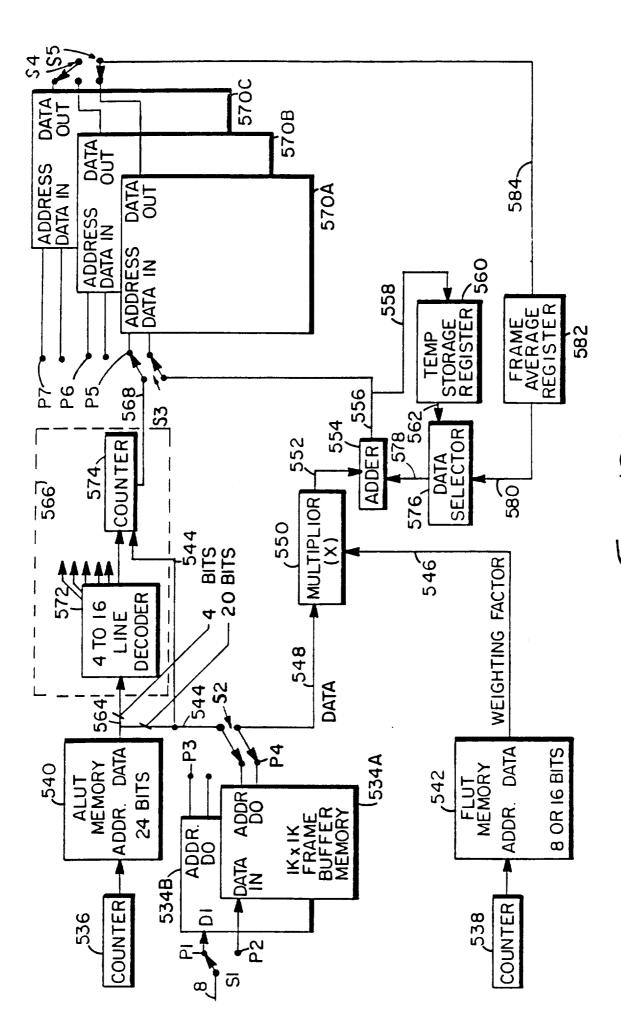
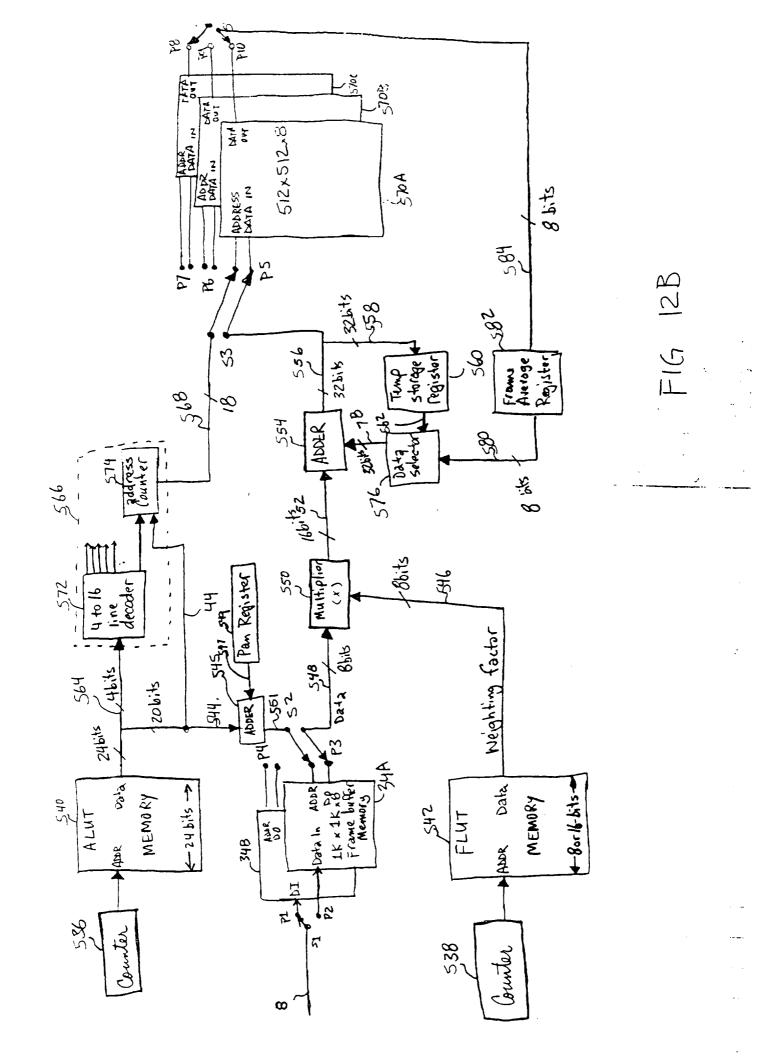


FIG. 12A



S .	ADDRESS		
I6 BITS	DESTINATION	ETC.	-

## FIG. 13A

I6 BITS	SOURCE (Xu,v,Yu,v) ADDR.	DESTINATION ADDRESS	ETC.	
1		L		

FIG. 14A

₩—16 BITS—	DEST. ADDR.	ETC.	BITS
►-20 BITS	SOURCE ADDR.	ETC.	<b>4</b> 36 B

FIG. 138

	0	0	0	-		
2I BITS	SOURCE ADDRESS	ADDRESS	•	SOURCE ADDRESS	ETC.	
- 21	SOURCE	SOURCE	•	SOURCE	Ш	
	-st	5nd		₽Z		

FIG. 148

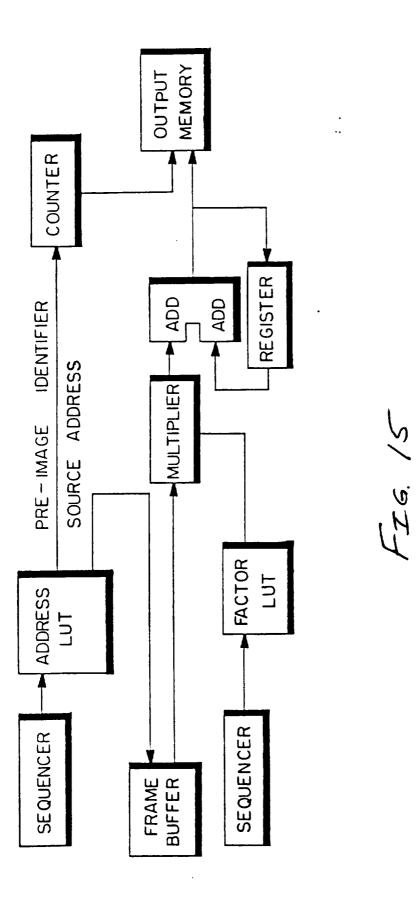
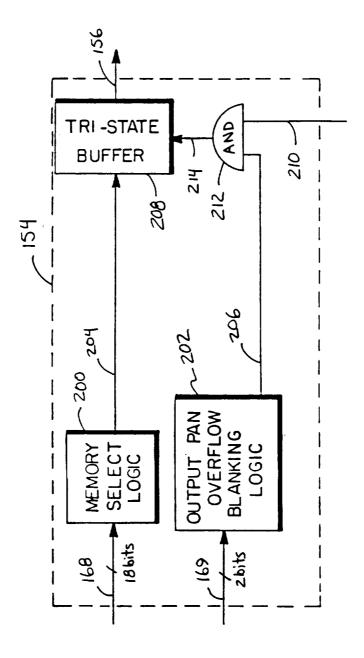
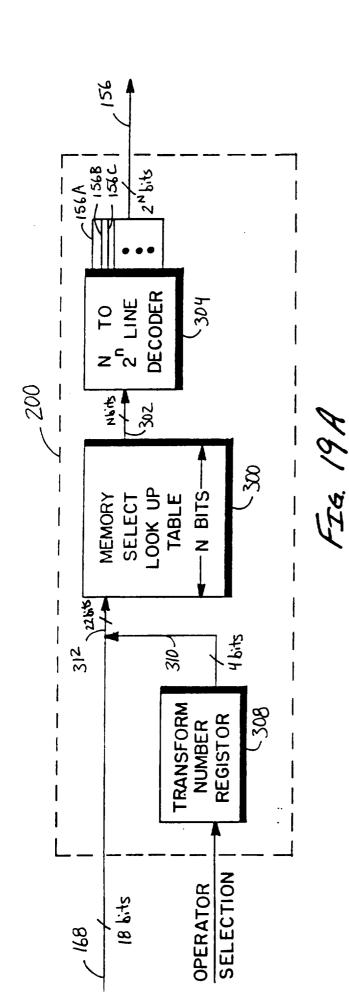


FIG. 16





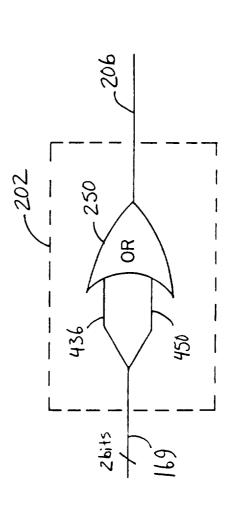


FIG. 18

